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PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10019056	04/22/2002	257		2811	T. TRAN

**APPLICANTS: Demizu Kiyoshi; Kato Tadahiro; Netsu Shigeyoshi;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A 371 OF PCT/JP01/03635 04/26/2001

YES TT

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 2000-128502 04/27/2000

YES TT

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Foreign priority claimed ☑ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiner's initials

ATTORNEY DOCKET NO
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TITLE : Semiconductor wafer and device for semiconductor device manufacturing process

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE	Application Examiner

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